भारतीय प्रौद्योगिकी संस्थान गोवा
गोवा अभियांत्रिकी महाविद्यालय परिसर, फार्मागुड़ी, फ़ोंडा – 403401, गोवा

Indian Institute of Technology Goa
Goa College of Engineering Campus, Farmagudi, Ponda – 403401, Goa

IITGoa/RECT/2024/02/TS(E)/704 Date: 31.01.2025

NOTICE

Sub: Selection Procedure
Name of the Post: Technical Superintendent - Electrical (PL 6; Group B)
Ref: Advt. No. IITGoa/RECT/2024/02 dated 04.10.2024

1. **Selection Will Be Based Performance in Written Test.**

2. **Pattern of the Written Test:**
   - The Written Test will be conducted in Two Stages, i.e. Written Test I and Written II. Candidates securing minimum qualifying marks as laid down by the selection committee in Written Test I shall be shortlisted for Written test II. The final selection will be based on aggregate marks obtained from both the Written Tests (I & II) with weightage of 40% in Written Test I and 60% in Written Test II.
   - Written Test I will Consist of 50 Multiple Choice Questions of 1 Marks Each. 0.25 Negative Marks for every wrong answer. Duration of the Test is 90 minutes.
   - Written Test II will be a Trade Test of 50 marks

3. **Syllabus:**
   Circuit Analysis: Node and Mesh Analysis, Superposition, Thevenin's Theorem, Norton's Theorem, Reciprocity. Sinusoidal Steady State Analysis: Phasors, Complex Power, Maximum Power Transfer. Time and Frequency Domain Analysis of Linear Circuits: RL, RC and RLC Circuits, Solution of Network Equations Using Laplace Transform. Linear 2-Port Network Parameters, Wye-Delta Transformation.

   Analog Circuits: Diode Circuits - Clipping, Clamping and Rectifiers. BJT and MOSFET Amplifiers - Biasing, AC Coupling, Small Signal Analysis, Frequency Response, Channel Length Modulation. Current Mirrors and Differential Amplifiers. Op-Amp Circuits: Amplifiers, Summers, Differentiators, Integrators, Active Filters, Schmitt Triggers and Oscillators. Feedback Topologies.

   Digital Circuits: Number Representations - Binary, Integer and Floating-Point- Numbers, Combinatorial Circuits - Boolean Algebra, Minimization of Functions Using Boolean Identities and Karnaugh Map, Logic Gates and Their Static CMOS Implementations, Arithmetic Circuits, Code Converters, Multiplexers, Decoders. Sequential Circuits - Latches and Flip-Flops, Counters, Shift-Registers, Finite State Machines, Propagation Delay, Setup and Hold Time, Critical Path Delay. Data Converters - Sample and Hold Circuits, ADCS and DACS. Semiconductor Memories - ROM, SRAM, DRAM. Computer Organization - Machine Instructions and Addressing Modes, ALU, Data-Path and Control Unit, Instruction Pipelining. Microprocessors and Microcontrollers.

   Power Electronics: Static V-I Characteristics And Firing/Gating Circuits For Thyristor, MOSFET, IGBT; DC To DC Conversion: Buck, Boost And Buck-Boost Converters; Single And Three-Phase Configuration Of Uncontrolled Rectifiers; Thyristor Based Converters; Bidirectional AC To DC Voltage Source Converters; Magnitude And Phase Of Line Current Harmonics For Uncontrolled And Thyristor Based Converters; Power Factor And Distortion Factor Of AC To DC Converters; Singlephase And Three-Phase Voltage Source Inverters, Sinusoidal Pulse Width Modulation.

4. **Date of Written Test:** Friday, 07/03/2025 at IIT Goa Campus 10:00 AM onwards

Sd/-
Registrar