INDIAN INSTITUTE OF TECHNOLOGY GOA

At Goa Engineering College Campus
Farmagudi, Ponda, Goa 403401
E-mail: purchase@iitgoa.ac.in

Enquiry No: IITGOA/2018-19/032 **Date: 30/11/2018**

IIT Goa invites sealed quotations in two bid format for the supply of below mentioned item.

Sl. No.	Description of Items	No. of Licences
1.	Cadence VLSI products - Research Bundle of Analog & Digital front-end and back end (Detailed specifications attached)	20 Licences for 3 years

Terms and conditions:

1. Quotation must be valid for at least 90 days.
2. The GSTIN should invariably be mentioned in your offer.
3. Price justification documents should be supplied along with the quote.
4. Warranty: 3 years (36 Months) from the date of successful installation, which includes free product updates and technical support.
5. Supplier should provide free installation service of the software for the change of installed licence server if required.
6. Supplier should organize one/two days workshop/training for the students and faculties at IIT Goa.
7. Prices should be quoted in Indian Rupees inclusive of any shipping charges.
8. The suppliers shall provide the banking details along with their quote on their letterhead duly signed and stamped.
9. Delivery and installation must be made within 4 weeks of getting a confirmed order.
10. Payment: Within 30 days after the delivery and successful installation.
11. IIT Goa reserves the right to accept and/or reject any/all bids without assigning any reason.
12. Quotations shall be submitted in two parts;
    1) **Part – I (Technical)** should contain all the technical details and specification of the product. It should contain unpriced bid along with terms and conditions, AMC, compliance certificates, Proprietary certificates (If applicable) etc. This envelope should be marked as "Technical Bid"
    2) **Part -II (Financial)** The financial bid of the above item should be in a sealed envelope marked as "Financial Bid" and should contain financial terms and conditions.
13) All sealed quotations must reach to the Assistant Registrar (Stores & Purchase), IIT Goa, at Goa College of Engineering Campus, Farmagudi, Ponda - Goa by 15.00 Hrs on or before 21st December, 2018".

Sd/-
Asst. Registrar (S&P)

Specifications

The research bundle should include licenses for the latest versions of the tools listed below.

VLSI tools for analog design

- Virtuoso(R) Schematic Editor XL
- Virtuoso Multi-mode Simulation with Spectre XPS
- Virtuoso(R) Analog Design Environment XL
- Virtuoso(R) Analog Design Environment GXL
- Virtuoso(R) Layout Suite GXL
- Virtuoso(R) Layout Suite XL
- AMS Designer with Flexible Analog Simulation
- Virtuoso AMS Designer Verification Option
- Cadence® Physical Verification System Design Rule Checker XL
- Cadence® Physical Verification System Layout vs. Schematic Checker XL
- Cadence Quantus QRC Extraction - XL
- Virtuoso Implementation Aware Design Option
- Virtuoso® RelXpert
- Virtuoso Accelerated Parallel Simulator
- Virtuoso Multi-mode Simulation Power option
- Virtuoso Multi-mode Simulation CPU Accelerator option
- Spectre Extensive Partitioned Simulator
- Spectre Characterization Simulator Option
- Virtuoso® Analog Oasis Run-Time Option
- Cadence(R) OASIS for RFDE
- Virtuoso(R) Schematic VHDL Interface
- Virtuoso(R) Schematic Editor Verilog(R) Interface
- Virtuoso(R) Analog HSPICE Interface Option
- Virtuoso Advanced Device Modeling HVMOS (For Eldo)
- Virtuoso Advanced Device Modeling HVMOS (For HSPICE)
- Pcell Generator
- Graphical Technology Editor
- Virtuoso Liberate Server
- Virtuoso Liberate Client
- Virtuoso Variety Server
- Virtuoso Variety Client
- Virtuoso Liberate MX Server
- Virtuoso Liberate MX Client
- Virtuoso Liberate LV Server
- Virtuoso Liberate LV Client
- Cadence Quantus QRC Advanced Analysis GXL option
- Cadence Quantus QRCX Display Technology Option
- Cadence® Quantus QRC Advanced Node Modeling Option

VLSI tools for digital design

- Incisive Enterprise Simulator - XL
- Genus Synthesis Solution
- Innovus Implementation System

- Genus Low Power Option
- Genus Physical Option
- Genus CPU Accelerator Option
- MODUS ATPG
- Modus Daignostics
- MODUS DFT Option
- Modus LBIST Option
- Modus MBIST Option
- Enterprise Simulator - XL Interface for MTI
- Enterprise Simulator - XL Interface for VCS
- Incisive™ Formal Verifier
- Incisive™ Enterprise Verifier - XL
- Digital Mixed Signal Option to IES
- Voltus IC Power Integrity Solution XL
- Voltus IC Power Integrity Solution Advanced Analysis GXL
- Tempus Timing Signoff Solution XL
- Tempus Timing Signoff Solution TSO
- Tempus Timing Signoff Solution MP
- Innovus 20/16/14nm Option
- Innovus Mixed Signal Option
- Innovus DFM Option

VLSI tools for packaging

- Cadence SiP Digital Architect - XL
- Cadence® SiP Layout - XL
- Cadence 3D Design Viewer
- Litho Physical Analyzer
- Litho Electrical Analyzer

VLSI tools for PCB desgin

- Allegro® PCB Librarian - XL
- Allegro(R) Physical Viewer
- Allegro PCB Designer
- Allegro PCB High-Speed Option
- Allegro PCB Miniaturization Option
- Allegro PCB Analog/RF option
- Allegro PCB Routing Option
- Allegro Design Authoring High-Speed Option
- Allegro FPGA system Planner option
- Allegro AMS Simulator SLPS interface
- Allegro® Sigrity SI base
- Allegro Sigrity PI Base
- Allegro Sigrity Power Aware SI option
- Power Integrity Sign off and Optimization Option
- Allegro Sigrity system Serial Link Option
- Allegro Sigrity Package Assessment and Extraction Option